E+TC | VI | CBCGS

19/12/18

Paper / Subject Code: 37006 / VLSI DESIGN

Time: 3 Hours **Marks: 80**

1] Question no.1 is **compulsory**
2] Attempt any **three** questions out of remaining questions
3] Assume **suitable data** if **required**
4] **Figures** to the **right** indicate marks.

Q. No. 1) Attempt any four from the following [20]

a) Draw VTC curve of static CMOS inverter and show all critical voltages (V_{IL}, V_{IH}, V_{OL}, V_{OH}, and V_{INV}) on the plot. Also show current drawn by CMOS inverter on VTC.
b) Explain any two short channel effects in MOS transistor.
c) What are advantages and disadvantages of dynamic CMOS logic circuit?
d) Implement 4:1 multiplexer using NMOS pass transistor logic.
e) Explain different CMOS clocking styles.

Q. No. 2)

a) Consider a CMOS inverter circuit with the following parameters:
$V_{DD} = 3.3V$ $V_{t0,n} = 0.6V$ $V_{t0,p} = -0.9V$
$K_n = 200\mu A/V^2$ $K_P = 80\mu A/V^2$

Calculate noise margins of the circuit. Consider $K_R = 2.5$. [10]

b) Implement $Y = \overline{A(B+C)(D+E)}$ using
(i) static CMOS logic style
(ii) Dynamic logic
(iii) Depletion load logic
(iv) Pseudo NMOS logic [10]

Q. No. 3)

a) Explain in detail the fabrication sequence of NMOS transistor with cross sectional view of each step. [10]

b) Draw schematic of six transistor SRAM cell. Describe various constraints that should be imposed on the devices to guarantee safe read and write operation. Also discuss relative sizing of the transistors in the cell. [10]

Q. No. 4)

a) Define scaling. Explain different types of scaling. [10]

b) Construct a full adder mirror circuit and compare the structure with direct static CMOS circuit. [10]

Q. No. 5)

a) What are different types of design rules? Draw layout of two input CMOS NAND gate as per lambda based design rules (show units in lambda). [10]

b) Explain in detail static and dynamic power dissipation, What are the main components which make power dissipation in CMOS circuit? [5]

c) What is clock skew? Explain clock distribution technique in VLSI system. [5]

Q. No.6) Write short notes on any FOUR [20]

i) ESD protection circuit.
ii) 4x4 Barrel shifter
iii) Latch up.
iv) 3-T DRAM
v) Decoder in memory structure

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